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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,704	02/13/2004	Yoshitaka Nakamura	Q79889	5693

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/777,704	NAKAMURA ET AL
	Examiner	Art Unit
	Thomas L. Dickey	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *4-7,10-14,17 and 21-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8,9,15,16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/10/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The preliminary amendment filed on 07/06/98 has been entered.

Election/Restriction

2. Applicants' election without traverse of Group I, claims 1-21 in the Paper filed 03/25/2005 is acknowledged.

3. Within the elected Group, on 08/01/2005 Applicants elected, without traverse, Embodiment I, figure 5, claims 1-3,8,9,15,16, and 18-20 (within the Group) readable thereon. This election of species is acknowledged.

Oath/Declaration

4. The oath/declaration filed on 08/10/2004 is acceptable.

Drawings

5. The formal drawings filed on 02/13/2004 are acceptable.

Priority

6. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

7. The Information Disclosure Statement filed on 08/10/2004 has been considered.

Specification

8. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 2,9,15,16, and 18-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 2 and 9, line 12, the expression " at least 30 nm or less" is indefinite because it recites a broad limitation (at least) and a narrow limitation (or less) within the broad limitation. Note that use of a narrower range within a broader range in the same claim renders the claim indefinite, since the resulting claims does not clearly set forth the metes and bounds of the patent protection desired. For examination purposes it will be assumed these claims simply recite "at least 30 nm."

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 1-3,8,9,15,16, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by AHN ET AL. (2003/0124812).

With regard to claims 1,15,16, and 18-20 Ahn et al. discloses a semiconductor device comprising memory cells each having a MISFET for memory selection formed on one major surface of a semiconductor substrate 11 and a capacitive element comprised of a metal ruthenium film lower electrode 29 electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a titanium nitride film first metal layer 21 and a ruthenium film upper electrode 35 formed on said lower electrode 29 via a titanium nitride (TiON, which includes titanium nitride and has an advantage over pure titanium nitride in that pure titanium nitride is conductive while TiON is insulative) capacitive insulating film 33, wherein said lower electrode 29 has a

thickness of 30 nm or greater at the bottom portion thereof. Note figures 7,10, and 11, and paragraphs 0018, 0021, 0026, 0028 of Ahn et al.

With regard to claims 2,15,16, and 18-20 Ahn et al. discloses a semiconductor device comprising memory cells each having a MISFET for memory selection formed on one major surface of a semiconductor substrate 11 and a capacitive element comprised of a metal ruthenium film lower electrode 29 electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a titanium nitride film first metal layer 21 and a ruthenium film upper electrode 35 formed on said lower electrode 29 via a titanium nitride (TiON, which includes titanium nitride and has an advantage over pure titanium nitride in that pure titanium nitride is conductive – pure titanium nitride cannot enable the claim – while TiON is insulative) capacitive insulating film 33, wherein said lower electrode 29 has a thickness of 30 nm or greater at the bottom portion thereof, and wherein said lower electrode 29 has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film 25. Note figures 7,10, and 11, and paragraphs 0018, 0021, 0026, 0028 of Ahn et al.

With regard to claims 3,15,16, and 18-20 Ahn et al. discloses a semiconductor device comprising memory cells each having a MISFET for memory selection formed on one major surface of a semiconductor substrate 11 and a capacitive element comprised of a metal ruthenium film lower electrode 29 electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a titanium nitride film first metal layer 21 and a ruthenium film upper electrode 35 formed on said lower

electrode 29 via a titanium nitride (TiON, which includes titanium nitride and has an advantage over pure titanium nitride in that pure titanium nitride is conductive while TiON is insulative) capacitive insulating film 33, wherein said lower electrode 29 has a thickness of 30 nm or greater at the bottom portion thereof, and wherein said lower electrode 29 has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film 25, and said lower electrode 29 has a thickness of at least 30 nm or less at a side portion thereof. Note figures 7,10, and 11, and paragraphs 0018, 0021, 0026, 0028 of Ahn et al.

With regard to claims 8,15,16, and 18-20 Ahn et al. discloses a semiconductor device comprising memory cells each having a MISFET for memory selection formed on one major surface of a semiconductor substrate 11 and a capacitive element comprised of a metal ruthenium film lower electrode 29 electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a titanium nitride film first metal layer 21 and a ruthenium film upper electrode 35 formed on said lower electrode 29 via a titanium nitride (TiON, which includes titanium nitride and has an advantage over pure titanium nitride in that pure titanium nitride is conductive while TiON is insulative) capacitive insulating film 33, wherein said lower electrode 29 has a thickness of 30 nm or greater at the bottom portion thereof, and wherein said lower electrode 29 has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film 25, and said lower electrode 29 has a thickness of at least 30 nm or less at a side portion thereof, further comprising a second metal

layer 19, wherein said first metal layer 21 and said second metal layer 19 partly contact each other, and said lower electrode 29 is connected at an entire bottom thereof to said second metal layer 19. Note figures 7,10, and 11, and paragraphs 0018, 0021, 0026, 0028 of Ahn et al.

With regard to claims 9,15,16, and 18-20 Ahn et al. discloses a semiconductor device comprising memory cells each having a MISFET for memory selection formed on one major surface of a semiconductor substrate 11 and a capacitive element comprised of a metal ruthenium film lower electrode 29 electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a titanium nitride film first metal layer 21 and a ruthenium film upper electrode 35 formed on said lower electrode 29 via a titanium nitride (TiON, which includes titanium nitride and has an advantage over pure titanium nitride in that pure titanium nitride is conductive while TiON is insulative) capacitive insulating film 33, wherein said lower electrode 29 has a thickness of 30 nm or greater at the bottom portion thereof, and wherein said lower electrode 29 has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film 25, and said lower electrode 29 has a thickness of at least 30 nm or less at a side portion thereof, further comprising a second metal layer 19, wherein said first metal layer 21 and said second metal layer 19 partly contact each other, and said lower electrode 29 is connected at an entire bottom thereof to said second metal layer 19. Note figures 7,10, and 11, and paragraphs 0018, 0021, 0026, 0028 of Ahn et al.

B. Claims 1-3,8,9,15, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by LANE (2002/0048870).

With regard to claims 1,15, and 20 Lane discloses a semiconductor device comprising memory cells each having a MISFET 30 for memory selection formed on one major surface of a semiconductor substrate 12 and a capacitive element comprised of a metal film lower electrode 70 (in figure 9 and paragraph 37, where the thickness is disclosed, the lower electrode 70 is identified as part 65) electrically connected at a bottom portion to one of a source and drain 16 of said MISFET 30 for memory selection via a first metal layer 60 and an upper electrode 74 formed on said lower electrode 70 via a capacitive insulating film 72, wherein said lower electrode 70 has a thickness of 30 nm or greater at the bottom portion thereof. Note figures 9 and 14, and paragraphs 37 and 39 of Lane.

With regard to claims 2,15, and 20 Lane discloses a semiconductor device comprising memory cells each having a MISFET 30 for memory selection formed on one major surface of a semiconductor substrate 12 and a capacitive element comprised of a metal film lower electrode 70 (in figure 9 and paragraph 37, where the thickness is disclosed, the lower electrode 70 is identified as part 65) electrically connected at a bottom portion to one of a source and drain 16 of said MISFET 30 for memory selection via a first metal layer 60 and an upper electrode 74 formed on said lower electrode 70 via a capacitive insulating film 72, wherein said lower electrode 70 has a thickness of 30 nm or greater at the bottom portion thereof, wherein said lower electrode 70 has a

shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film 25. Note figures 9 and 14, and paragraphs 37 and 39 of Lane.

With regard to claims 3,15, and 20 Lane discloses a semiconductor device comprising memory cells each having a MISFET 30 for memory selection formed on one major surface of a semiconductor substrate 12 and a capacitive element comprised of a metal film lower electrode 70 (in figure 9 and paragraph 37, where the thickness is disclosed, the lower electrode 70 is identified as part 65) electrically connected at a bottom portion to one of a source and drain 16 of said MISFET 30 for memory selection via a first metal layer 60 and an upper electrode 74 formed on said lower electrode 70 via a capacitive insulating film 72, wherein said lower electrode 70 has a thickness of 30 nm or greater at the bottom portion thereof, wherein said lower electrode 70 has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film 25, and wherein said lower electrode 70 has a thickness of at least 30 nm or less at a side portion thereof. Note figures 9 and 14, and paragraphs 37 and 39 of Lane.

With regard to claims 8,15, and 20 Lane discloses a semiconductor device comprising memory cells each having a MISFET 30 for memory selection formed on one major surface of a semiconductor substrate 12 and a capacitive element comprised of a metal film lower electrode 70 (in figure 9 and paragraph 37, where the thickness is disclosed, the lower electrode 70 is identified as part 65) electrically connected at a bottom portion to one of a source and drain 16 of said MISFET 30 for memory selection

via a first metal layer 60 and an upper electrode 74 formed on said lower electrode 70 via a capacitive insulating film 72, wherein said lower electrode 70 has a thickness of 30 nm or greater at the bottom portion thereof, wherein said lower electrode 70 has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film 25. Note figures 9 and 14, and paragraphs 37 and 39 of Lane, and further comprising a second metal layer 52, wherein said first metal layer 60 and said second metal layer 52 partly contact each other, and said lower electrode 70 is connected at an entire bottom thereof to said second metal layer 52. Note figures 9 and 14, and paragraphs 37 and 39 of Lane.

With regard to claims 9,15, and 20 Lane discloses a semiconductor device comprising memory cells each having a MISFET 30 for memory selection formed on one major surface of a semiconductor substrate 12 and a capacitive element comprised of a metal film lower electrode 70 (in figure 9 and paragraph 37, where the thickness is disclosed, the lower electrode 70 is identified as part 65) electrically connected at a bottom portion to one of a source and drain 16 of said MISFET 30 for memory selection via a first metal layer 60 and an upper electrode 74 formed on said lower electrode 70 via a capacitive insulating film 72, wherein said lower electrode 70 has a thickness of 30 nm or greater at the bottom portion thereof, wherein said lower electrode 70 has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film 25, and wherein said lower electrode 70 has a thickness of at least 30 nm or less at a side portion thereof, and further comprising a second metal layer 52,

wherein said first metal layer 60 and said second metal layer 52 partly contact each other, and said lower electrode 70 is connected at an entire bottom thereof to said second metal layer 52. Note figures 9 and 14, and paragraphs 37 and 39 of Lane.

C. Claims 1-3,15,16, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by LEE ET AL. (2002/0052126).

With regard to claims 1,15,16, and 19 Lee et al. discloses a semiconductor device comprising memory cells each having a MISFET 31 (or 32,33, or 34) for memory selection formed on one major surface of a semiconductor substrate 20 and a capacitive element 86 (or 87) comprised of a ruthenium metal film lower electrode 73 electrically connected at a bottom portion to one of a source and drain 26 of said MISFET 31 for memory selection via a first metal layer 52 and a ruthenium film upper electrode 74 formed on said lower electrode 73 via a capacitive insulating film 72, wherein said lower electrode 73 has a thickness of thirty nm or greater at the bottom portion thereof. Note figure 12 and paragraphs 27,28, and 41-44 of Lee et al.

With regard to claims 2,1,15,16, and 19 Lee et al. discloses a semiconductor device comprising memory cells each having a MISFET 31 (or 32,33, or 34) for memory selection formed on one major surface of a semiconductor substrate 20 and a capacitive element 86 (or 87) comprised of a ruthenium metal film lower electrode 73 electrically connected at a bottom portion to one of a source and drain 26 of said MISFET 31 for memory selection via a first metal layer 52 and a ruthenium film upper electrode 74 formed on said lower electrode 73 via a capacitive insulating film 72,

wherein said lower electrode 73 has a thickness of thirty nm or greater at the bottom portion thereof, wherein said lower electrode 73 has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film 60. Note figure 12 and paragraphs 27,28, and 41-44 of Lee et al.

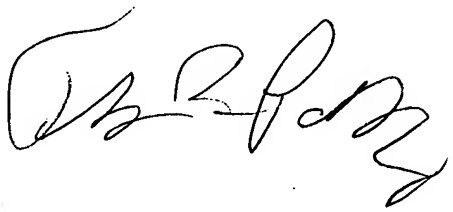
With regard to claims 3,1,15,16, and 19 Lee et al. discloses a semiconductor device comprising memory cells each having a MISFET 31 (or 32,33, or 34) for memory selection formed on one major surface of a semiconductor substrate 20 and a capacitive element 86 (or 87) comprised of a ruthenium metal film lower electrode 73 electrically connected at a bottom portion to one of a source and drain 26 of said MISFET 31 for memory selection via a first metal layer 52 and a ruthenium film upper electrode 74 formed on said lower electrode 73 via a capacitive insulating film 72, wherein said lower electrode 73 has a thickness of thirty nm or greater at the bottom portion thereof, wherein said lower electrode 73 has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film 60, and wherein said lower electrode 73 has a thickness of at least thirty nm or less at a side portion thereof. Note figure 12 and paragraphs 27,28, and 41-44 of Lee et al.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
08/05